

APPENDIX G

An output of even odd receiver 306 at node 308 is coupled to an input of a shift register comprising flip-flops 314, 316, 318, and 320. A receive clock is provided to a clock input of the shift register at node 310. An unload signal for providing parallel data outputs from the shift register is applied to the shift register via node 312. Parallel data are provided at parallel data outputs 322, 324, 326, and 328 of flip-flops 314, 316, 318, and 320, respectively.